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YEUNG LOPEZ, FEIFEI	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/567,883	STEIN ET AL.	
	Examiner	Art Unit	
	FEI FEI YEUNG LOPEZ	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34 and 42-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34 and 42-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *6/13/08; 6/24/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-13,16-17,19,21-22,25,28-29,33,45-46, and 48-49 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al (PG Pub 2002/0137244 A1) in view of Noto et al (WO/2002/061855).

4. Regarding claim 1, Chen teaches a radiation-emitting semiconductor component comprising: a semiconductor body that includes a first principal surface (top surface of layer 116 in fig. 1), a second principal surface (bottom surface of layer 112) and an epitaxially formed semiconductor layer sequence (layers 112,114, and 116) with an electromagnetic radiation generating active zone, said epitaxially formed semiconductor layer sequence forming the semiconductor body and being disposed between the first and the second principal surfaces; a first current spreading layer (layer 118) and a

second non-epitaxially formed current spreading layer (ITO layer, see paragraph [0037]) disposed on said second principal surface and electrically conductively connected to said semiconductor layer sequence. However, Chen does not teach that the first current spreading layers is non-epitaxially formed. In the same field of endeavor, Noto teaches a first non-epitaxially formed current spreading layer (top ITO layer infig. 1) disposed on a first principal surface and electrically conductively connected to a semiconductor layer sequence; and a second non-epitaxially formed current spreading layer (bottom ITO layer) disposed on a second principal surface and electrically conductively connected to said semiconductor layer sequence for the benefit of distributing current in desired areas. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include a first non-epitaxially formed current spreading layer disposed on a first principal surface and electrically conductively connected to a semiconductor layer sequence; and a second non-epitaxially formed current spreading layer disposed on a second principal surface and electrically conductively connected to said semiconductor layer sequence for the benefit of distributing current in desired areas.

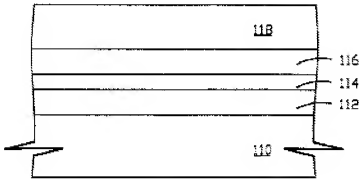


FIG.1(PRIOR ART)

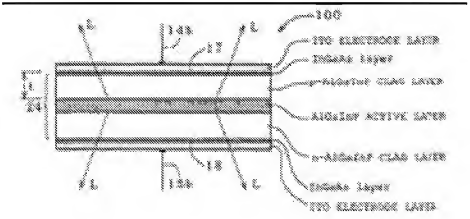


Fig. 1 of Noto et al

5. Regarding claim 2, Chen teaches the radiation-emitting semiconductor component as in claim 1, wherein at least one of said two principal surfaces comprising said current spreading layers has a microstructure (in paragraph [0038], Chen teaches

roughening the surface between a current spreading layer (ohmic electrode layer 68 in fig. 6), the roughened surface forms a microstructure).

6. Regarding claim 3, Chen teaches the radiation-emitting semiconductor component as in claim 1, wherein at least one of said current spreading layers contains a material that is transparent to the generated radiation (paragraph [0007] and ITO layer, see paragraph [0038]).

7. Regarding claim 4, Noto teaches the radiation-emitting semiconductor component as in claim 2, wherein both current spreading layers contain a material that is transparent to the generated radiation (ITO, see abstract).

8. Regarding claim 5, Chen and Noto teach the radiation-emitting semiconductor component as in claim 3, wherein-said radiation-transparent material contains an oxide (ITO layer, see paragraph [0038] of Chen and fig. 1 of Noto).

9. Regarding claim 6, Chen and Noto teach the radiation-emitting semiconductor component as in claim 5, wherein said oxide is a metal oxide (ITO layer).

10. Regarding claim 7, Chen and Noto teach the radiation-emitting semiconductor component as in claim 3, wherein said radiation-transparent material contains ITO and/or InO.

11. Regarding claim 8, Chen teaches the radiation-emitting semiconductor component as in claim 3, wherein-said radiation-transparent material contains ZnO (paragraph [0038]).

12. Regarding claim 9, Chen teaches the radiation-emitting semiconductor component as in claim 3, wherein said radiation-transparent material contains SnO (paragraph [0038]).

13. Regarding claim 10, Chen teaches the radiation-emitting semiconductor component as in claim 1, wherein at least one of said current spreading layers contains A1, Ga, In, Ce, Sb and/or F (AlGa layer 118 in fig. 1).

14. Regarding claim 11, Chen teaches the radiation-emitting semiconductor component as in claim 1, wherein disposed on at least one of said current spreading layers is a mirror layer (DBR between LED epitaxial layer and substrate, see paragraph [0008]).

15. Regarding claim 12, Chen teaches the radiation-emitting semiconductor component as in claim 11, wherein said mirror layer is disposed on the side of said current spreading layer facing away from said semiconductor layer sequence (DBR between LED epitaxial layer and substrate, see paragraph [0008]).

16. Regarding claim 13, Chen teaches the radiation-emitting semiconductor component as in claim 11, wherein said mirror layer is electrically conductive (note that the DBR must be conductive for there to be electricity flowing through the DBR from ohmic electrode 68 to the active layer 64, see fig. 6).

17. Regarding claim 16, Chen teaches the radiation-emitting semiconductor component as in claim 11, wherein said principal surface has a microstructure on the side of said semiconductor layer sequence facing away from said mirror layer (in

paragraph [0038], Chen teaches roughening the surface between a current spreading layer (ohmic electrode layer 68 in fig. 6), the roughened surface forms a microstructure).

18. Regarding claim 17, Chen teaches the radiation-emitting semiconductor component as in claim 1, wherein said semiconductor layer sequence contains at least one n- and/or p-conductive layer (p layer 116 or n layer 112 in fig. 1).

19. Regarding claim 19, Chen and Noto teach the radiation-emitting semiconductor component as in claim 17 wherein the current spreading layer on the side comprising the p-conductive layer of the semiconductor layer sequence contains ZnO and preferably Al. Note that Chen teaches using AlGaAs as a current spreading layer (layer 78) and adding and ITO between layers 66 and 68 (paragraph [0038]). Noto teaches using current spreading layer on both top and bottom surfaces of a semiconductor device. One of ordinary skill would have been motivated to include AlGaAs current spreading layer on the top and the bottom surfaces on the semiconductor device and to include an ITO layer between layers 66 and 68, as disclosed by Chen.

20. Regarding claim 21, Chen teaches the radiation-emitting semiconductor component as in claim 1, wherein said radiation-emitting semiconductor component is affixed to a carrier (GaAs substrate 110 in fig. 1).

21. Regarding claim 22, Chen teaches the radiation-emitting semiconductor component as in claim 21, wherein said carrier contains GaAs (GaAs substrate 110 in fig. 1).

22. Regarding claim 25, Chen teaches the radiation-emitting semiconductor component as in claim 1, wherein disposed on at least one of the first current spreading

layer and the second current spreading layer is a contact surface for electrical contacting (ohmic electrode disposed on ITO layer, see fig. 6 and paragraph [0038]).

23. Regarding claim 28, Chen teaches the radiation-emitting semiconductor component as in claim 1, wherein at least one of said current spreading layers comprises a recess (recess formed between current spreading layer 62 in fig. 6).

24. Regarding claim 29, Chen teaches the radiation-emitting semiconductor component as in claim 28, wherein disposed in said recess is an electrically conductive contact surface (surface of layer 68 in fig. 6).

25. Regarding claim 33, Chen teaches the radiation-emitting semiconductor component as in claim 1, wherein said semiconductor layer sequence contains a II1/V semiconductor, preferably $In_xGa_yAl_{1-x-y}As$ (layer 116 in fig. 1), where $0 \leq x \leq 1$.

26. Regarding claim 45, Noto teaches the radiation-emitting semiconductor component as in claim 1, wherein the first current spreading layer and the second current spreading layer contain an oxide (ITO layers, see fig. 1).

27. Regarding claim 46, Chen teaches the radiation-emitting semiconductor component as in claim 1, wherein the first current spreading layer comprises a first material and the second current spreading layer comprises a second material different from the first material (layer 62 in fig. 6 and ITO layer in paragraph [0038]).

28. Regarding claim 48, Chen teaches the epitaxially formed semiconductor layer sequence. Noto teaches a lattice mismatch at a first principal surface between the a semiconductor layer sequence and a first non-epitaxially formed current spreading layer (ITO layer on top in fig. 1), and further comprising a lattice mismatch at a second

principal surface between the semiconductor layer sequence and second non-epitaxially formed current spreading layer (ITO layer on the bottom in fig. 1).

29. Regarding claim 49, Chen teaches a radiation-emitting semiconductor component comprising: a semiconductor body that includes a first principal surface (top surface of layer 116 in fig. 1), a second principal surface (bottom surface of layer 112) and an epitaxially formed semiconductor layer sequence (layers 112,114, and 116) with an electromagnetic radiation generating active zone, said epitaxially formed semiconductor layer sequence forming the semiconductor body and being disposed between the first and the second principal surfaces; a first current spreading layer (layer 118) and a second non-epitaxially formed current spreading layer (ITO layer, see paragraph [0037]) disposed on said second principal surface and electrically conductively connected to said semiconductor layer sequence. However, Chen does not teach that the first current spreading layer is a metal oxide layer, and Chen does not teach that the first current spreading layer is non-epitaxially formed. In the same field of endeavor, Noto teaches a first non-epitaxially formed metal oxide current spreading layer (top ITO layer in fig. 1) disposed on a first principal surface and electrically conductively connected to a semiconductor layer sequence; and a second non-epitaxially formed metal oxide current spreading layer (bottom ITO layer) disposed on a second principal surface and electrically conductively connected to said semiconductor layer sequence for the benefit of distributing current in desired areas. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include a first non-epitaxially formed metal oxide current spreading layer disposed on a

first principal surface and electrically conductively connected to a semiconductor layer sequence; and a second non-epitaxially formed metal oxide current spreading layer disposed on a second principal surface and electrically conductively connected to said semiconductor layer sequence for the benefit of distributing current in desired areas.

30. Claims 14-15 and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al (PG Pub 2002/0137244 A1) in view of Noto et al (WO/2002/061855) as applied to claims 11 and 25 above, and further in view of Dutta et al (US Patent 5,861,636).

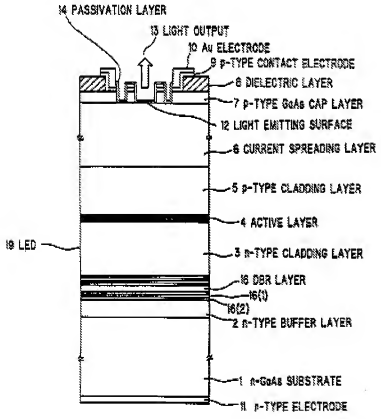
31. Regarding claim 14, the previous combination remains as applied in claim 11 above. However, the previous combination does not teach that said mirror layer contains a metal. In the same field of endeavor, Dutta teaches a mirror layer contains a metal (DBR material in table 1) for the benefit of high reflectivity. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include metal in said mirror layer for the benefit of high reflectivity.

32. Regarding claim 15, the previous combination remains as applied in claim 11 above. However, the previous combination does not teach said mirror layer contains Au, Ag, A1 and/or Pt. Dutta teaches said mirror layer contains Au, Ag, A1 and/or Pt (table 1).

33. Regarding claim 26, the previous combination remains as applied in claim 25 above. However, the previous combination does not teach that said contact surface is disposed on the side of said semiconductor layer sequence opposite to said carrier.

Dutta teaches a contact surface (contact electrode 9 in fig. 7) is disposed on the side of a semiconductor layer sequence opposite to a carrier (substrate 1).

FIG. 7



34. Regarding claim 27, the previous combination remains as applied in claim 25 above. However, the previous combination does not teach that said contact surface has on the side facing said semiconductor layer sequence a layer that reflects the generated radiation. Dutta teaches said contact surface has on the side facing said

semiconductor layer sequence a layer (Au electrode layer in fig. 7) that reflects the generated radiation.

35. Claims 18 and 42-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al (PG Pub 2002/0137244 A1) in view of Noto et al (WO/2002/061855) as applied to claim 17 above, and further in view of Kneissl et al (US Patent 6,515,308 B1).

36. Regarding claim 18, the previous combination remains as applied in claim 25 above. However, the previous combination does not teach that the thickness of said n-conductive and/or said p-conductive layer is in the range of a monolayer to 1000 nm. In the same field of endeavor, Kneissl teach that the thickness of an n-conductive and/or a p-conductive layer is in the range of a monolayer to 1000 nm (column 5, lines 19-23). Also note that discovery of an optimum range is well within the level of ordinary skill in the art, and such ranges will not support patentability unless there is evidence of its criticality. In re Aler, 220 F.2d 454.456.

37. Regarding claim 42, the previous combination remains as applied in claim 25 above. However, the previous combination does not teach that the thickness of said n-conductive and/or said p-conductive layer is less than 400 nm. Kneissl teach that the thickness of an n-conductive and/or a p-conductive layer is less than 400 nm (layer 118 in fig. 1, column 5, lines 19-23). Also note that discovery of an optimum range is well within the level of ordinary skill in the art, and such ranges will not support patentability unless there is evidence of its criticality. In re Aler, 220 F.2d 454.456.

38. Regarding claim 43, the previous combination remains as applied in claim 25 above. However, the previous combination does not teach that the thickness of said n-

conductive and/or said p-conductive layer is between 150 nm and 400 nm. Kneissl teach that the thickness of an n-conductive and/or a p-conductive layer is between 150 nm and 400 nm (n layer 108, see column 4, lines 59-61).

39. Claims 20 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al (PG Pub 2002/0137244 A1) in view of Noto et al (WO/2002/061855) as applied to claim 17 above, and further in view of Tran (US Patent 5,397,920).

40. Regarding claim 20, the previous combination remains as applied in claim 17 above. However, the previous combination does not teach that the current spreading layer on the side comprising the n-conductive layer of the semiconductor layer sequence contains SnO. In the same field of endeavor, Tran teaches a current spreading layer contains SnO (column 2, lines 14-20) for the benefit of decreased resistivity. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include SnO in the current spreading layer on the side comprising the n-conductive layer of the semiconductor layer sequence for the benefit of decreased resistivity.

41. Regarding claim 44, the previous combination remains as applied in claim 17 above. However, the previous combination does not teach that the current spreading layer on the side comprising the n-conductive layer of the semiconductor layer sequence contains SnO and Sb. In the same field of endeavor, Tran teaches a current spreading layer contains SnO and Sb (column 2, lines 14-20).

42. Claims 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al (PG Pub 2002/0137244 A1) in view of Noto et al (WO/2002/061855) as

applied to claims 21 and 1 above, and further in view of Shimanuki (PG Pub 2003/0001249 A1).

43. Regarding claim 23, the previous combination remains as applied in claim 21 above. However, the previous combination does not teach that said radiation-emitting semiconductor component is affixed to said carrier by means of a solder metallization. In the same field of endeavor, Shimanuki teaches a radiation-emitting semiconductor component is affixed to said carrier by means of a solder metallization for the benefit of improve mountubility (paragraph [0119]). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to affix the radiation-emitting semiconductor component to said carrier by means of a solder metallization for the benefit of improve mountubility. Note that "solder metallization is a process by which the product is made and is a process that does not carry patentable weight in a product claim. "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). See MPEP 2113.

44. Regarding claim 24, the previous combination remains as applied in claim 1 above. However, the previous combination does not teach that a solder metallization is disposed on said mirror layer to affix said radiation-emitting semiconductor component

to a carrier. Shimanuki teaches using a solder metallization to affix a semiconductor component to a carrier (paragraph [0119]).

45. Claims 28-32, 34, and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al (PG Pub 2002/0137244 A1) in view of Noto et al (WO/2002/061855) as applied to claim 1 above, and further in view of Rennie et al (US Patent 5,889,295).

46. Regarding claim 28, the previous combination remains as applied in claim 1. Additionally, and in the same field of endeavor, Rennie teaches a current spreading layer comprises a recess (see the top and the sides of layer 12 in fig. 5) for the benefit of reduced operating voltage (column 3, lines 29-38). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to include a recess in the current spreading layer for the benefit of reduced operating voltage.

47. Regarding claim 29, the previous combination remains as applied in claim 1. Additionally, Rennie teaches that disposed in said recess is an electrically conductive contact surface (see fig. 5, surface around layer 12).

48. Regarding claim 30, the previous combination remains as applied in claim 1. However, the previous combination does not teach that the electrical contacting of said radiation-emitting semiconductor component takes place via said contact surface. Rennie teaches that an electrical contacting of a radiation-emitting semiconductor component takes place via said contact surface (from layer 13 to layer 12, see fig. 5).

49. Regarding claim 31, the previous combination remains as applied in claim 1. However, the previous combination does not teach disposed on the side of said current

spreading layer facing said semiconductor layer sequence and provided with said recess and said contact surface is a jacket layer or a jacket layer sequence. Rennie teaches disposed on the side of said current spreading layer facing said semiconductor layer sequence and provided with said recess and said contact surface is a jacket layer (SiO_2 layer 11 in fig. 5) or a jacket layer sequence.

50. Regarding claim 32, the previous combination remains as applied in claim 1. However, the previous combination does not teach said jacket layer or jacket layer sequence is poorly electrically conductive with respect to said contact surface, such that the current partially flows into said current spreading layer. Rennie teaches said jacket layer (layer 11 in fig. 5) or jacket layer sequence is poorly electrically conductive with respect to said contact surface, such that the current partially flows into said current spreading layer (layer 12).

51. Regarding claim 34, previous combination remains as applied in claim 1. Furthermore, Chen teaches on the side nearest said semiconductor body of said first current spreading layer (layer 118 in fig. 1) adjoins a p-conductive AlGaAs-containing layer (layer 116 in fig. 1). However, the previous combination does not teach said first current spreading layer contains ZnO. Rennie teaches a current spreading layer contains ZnO (layer 12 in fig. 5).

52. Regarding claim 47, previous combination remains as applied in claim 1. However, the previous combination does not teach the first current spreading layer and the second current spreading layer are sputtered layers. Rennie teaches a first current

spreading layer (layer 12 in fig. 5) and a second current spreading layer (layer 2) are sputtered layers (column 4, lines 52-55).

Response to Arguments

53. Applicant's arguments with respect to claims 1-34 and 42-49 have been considered but are moot in view of the new ground(s) of rejection. Amendments to claim 1 raise new issues to claim 43 therefore this Office Action is properly made final even with new grounds of rejection.

Conclusion

54. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to FEI FEI YEUNG LOPEZ whose telephone number is

(571)270-1882. The examiner can normally be reached on 7:30am-5:00pm Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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